REMARKS

Claims 1-15 are currently active.

The Examiner has objected to Claims 2-8 and 10-15.

The Examiner has rejected Claims 1 and 9 as being unpatentable over Gorshe in view of Arslan. Applicant respectfully traverses this rejection. There is no teaching or suggestion in the applied art of record of any port card which performs parity calculations.

The Examiner on page 2 of the Office Action states that Gorshe teaches a port card (element 10). The Examiner goes on and states that bytes of data flowing into the interface unit are input immediately into the input port data latches 30, 32 which receive data through their respective input ports 10 and 12. However, in the previous paragraph of the Office Action, the Examiner states that elements 30 and 32 are parity fabrics. The Examiner cannot use the same element as both a parity fabric and as a port card. The claimed invention has two distinct elements, where one element is a parity fabric and a separate element is a port card. Furthermore, the limitation in Claim 1 clearly states that "the first port card performs first parity calculations on the data received at the first port card, produces first parity data from the first parity calculations and sends the fabric to the first parity data to or receive the data from the parity fabric at the connection rate".

Gorshe teaches that bytes of data flowing into the interface unit are input immediately into the input port data latches 30, 32 which receive data through their respective input ports 10 and 12, and which produce the first batch outputs corresponding to the data at the inputs upon receiving a pulse. These latches also each contain a parity check circuit which provides indications that the parity error input that parity errors occurred. The input port data latches 30, 32 consist of D-type latches in addition to two bytes wide parity calculations circuits. Parity errors are passed to the microprocessor interface for alarm reporting and summation. The parity calculations can be masked by software provisioning in support of the transfer configuration. See column 7, lines 28-46. As is clear from this teaching, input port data latches 30, 32 are distinct from the input port and that no parity calculation occurs at the input port. In this interpretation, the limitations of Claim 1 are not met.

If the Examiner takes the position that input port data latches 30, 32 are part of the input port 10, then there is no parity fabric, and by this interpretation limitations of the claim are not met.

Arslan does not teach or suggest parity calculations whatsoever. Accordingly, the applied art of record fails to teach or suggest a significant limitation in Claim 1 and in Claim 9. Claims 1 and 9 are patentable over the applied art of record.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-15, now in this application be allowed.

CERTIFICATE OF MAILING

I hereby certify that the correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on 10/19/04

Ansel M. Schwartz
Registration No. 30,587

10/19/04
Date

Respectfully submitted,

JEFF SCHULZ

By _____

Ansel M. Schwartz, Esquire
Reg. No. 30,587
One Sterling Plaza
201 N. Craig Street
Suite 304
Pittsburgh, PA 15213
(412) 621-9222

Attorney for Applicant